Page 3, amend the paragraph beginning at line 18 as follows:

Any other modulation scheme for symbol coding can be utilized, including quadrature amplitude modulation (QAM). In QAM schemes, for example, the symbols are arranged on a two-dimensional (real and imaginary) symbol constellation ~~constellations~~ (instead of the one-dimensional ~~one-dimension~~ constellations of the PAM-5 and ~~or~~ MLT-3 symbol alphabets).

Page 3, amend the paragraph beginning at line 24 as follows:

There is a need for transmitters and receivers for receiving transmission over multiple twisted copper pairs ~~pair~~ using larger symbol alphabets (i.e., 3 or more symbols). There is also a need for transceiver (transmitter/receiver) systems that, while operating at high symbol rates, have low bit error rates.

Page 3, amend the paragraph beginning at line 33 as follows:

Accordingly, a receiver and detection method for receiving transmission of data over multiple wires using encoded data symbol schemes having multiple symbols is described. A receiver according to the present invention includes multiple detectors for detecting one symbol from each of the multiple wires simultaneously (i.e., multiple 1-D detectors), an equalizer coupled to each of the detectors for equalizing the symbol stream from each of the multiple wires, and a multi-dimensional error analyzer/decoder for simultaneously making hard decisions ~~decision~~ regarding the symbol output of the symbols transmitted over each of the multiple wires.

Page 4, amend the paragraph beginning at line 10 as follows:

Individual symbols can have any modulation scheme, including those with multi-dimensional constellations. The terminology of detecting N-dimensional (N-D) symbols refers to the number of individual symbols detected in each clock cycle, and not to the dimension of the symbol constellation.

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Page 4, amend the paragraph beginning at line 32 as follows:

Some embodiments of the invention can also include an error analysis decoder. The receiver receives signals from N individual wires and, for each wire, includes a linear equalizer in combination with a one-dimensional (1-D) ~~a 1-D~~ sequence detector. The N output signals from the N 1-D sequence detectors are input to a N-D decoder that makes a final decision on the N-D symbol. In some embodiments of the invention, the error analysis decoder operates with lattice encoding schemes. In some other embodiments of the invention, the error analysis decoder operates with a parity encoding scheme.

Page 5, amend the paragraph beginning at line 19 as follows:

Figure 3 shows a trellis diagram for state transitions among subsets of PAM-5 four-dimensional (4-D) symbols. ~~4D symbols.~~

Page 7, amend the paragraph beginning at line 13 as follows:

Figure 1 shows a block diagram of a transceiver system 100 according to the present invention. Transceiver system 100 includes transmitter 101, receiver 107, and transport wires 103-1 through 103-N. A digital data stream is input to transmitter 101 by a first host 150. Transmitter 101 includes encoder 102, which encodes the data for transmission over transport wires 103-1 through 103-N. Transmission coupler 112 couples the encoded symbols received from encoder 102 to transmission channel 104. Data is output by transmission coupler 112 as symbols $a_{k,1}$ through $a_{k,N}$ over wires 103-1 through 103-N (collectively ~~103-N, (collectively~~ referred to as cable 103), respectively, which are coupled between transmitter 101 and receiver system 107. Wires 103-1 through 103-N can be of any transport medium or combination of transport media. Transport media include, for example, category-5 twisted copper pair, optical fiber and coax cable.

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Page 8, amend the paragraph beginning at line 4 as follows:

Transmission channel 104 collectively represents cable 103 and any distortion of the signals that occurs between transmitter 101 and a receiver 107. Each of wires 103-1 through 103-N, along with output couplers of coupler 112 and input couplers of detector 108, distorts ~~distort~~ signals as indicated by the associated transmission channel 104-1 through 104-N,

respectively. The signals through wires 103-1 through 103-N are distorted by channel functions $f_1(Z)$ through $f_N(Z)$, respectively, and additionally suffer from a random noise addition $n_{k,1}$ through $n_{k,N}$, respectively. Receiver 107 includes signal ~~includes a signal~~ detector 108 and a decoder 109 and ultimately outputs a data stream which corresponds to the data stream entering transmitter 101.

Page 8, amend the paragraph beginning at line 18 as follows:

In Gigabit Ethernet, transmission can be conducted on four twisted copper pairs (i.e., wires 103-1 through 103-4 in Figure 1) in a full duplex fashion to achieve one gigabit per second throughput. See IEEE 802.3ab, Gigabit Long Haul Copper Physical Layer Standards Committee, 1997 (hereinafter "Gigabit Standard"). Transmitter 101 is coupled to first ~~to a first~~ host 150 to receive data for transmission over transmission channel 104 to a second host 151 coupled to receiver 107. In general, first host 150 is further coupled to a receiver 111 for receiving data from transmission channel 104 and second host 151 is coupled to a transmitter 110 for sending data to transmission channel 104.

Page 8, amend the paragraph beginning at line 32 as follows:

Although, in general, the detection system as described here is applicable to any scheme of data transmission (i.e., any symbol alphabet) over any number of transport wires (e.g., twisted copper pair), for exemplary purposes many of the examples below specifically describe a PAM-5 symbol alphabet transmitted over four twisted copper pairs, ~~pair,~~ as would be used in Gigabit Ethernet transmission over Category-5 twisted pair cabling. It should be recognized that other symbol alphabets and numbers of conductors can also be used and that one skilled in the art will recognize from this disclosure embodiments appropriate for other modulation schemes.

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Page 9, amend the paragraph beginning at line 13 as follows:

According to the developed IEEE 802.3ab standard for Gigabit Ethernet transmission, the transmitted symbols on each of four conductors 103-1 through 103-4 are chosen from a five level Pulse Amplitude Modulation (PAM-5) constellation, with alphabet {A}={-2, -1, 0, +1, +2}. *See* Gigabit Standard. At each clock cycle, a single one-dimensional (1-D) symbol

is transmitted on each wire. The four 1-D symbols, one on each of conductors 103-1 through 103-4, transmitted at a particular sample time k are ~~k, is~~ considered to be a single 4-D symbol. In general, data entering transmitter 101 can be encoded into a N-D symbol, instead of into N 1-D symbols, by encoder 102. Encoder 102 may be any type of N-D encoder, including a N-D parity code encoder and a N-D trellis code encoder.

Page 10, amend the paragraph beginning at line 24 as follows:

The Gigabit Ethernet standard (see Gigabit Standard) ~~, *See Gigabit Standard,*~~ allows a trellis code. However, both a 4-D eight state trellis code and a 4-D parity code have been proposed. The trellis code achieves 6dB of coding gain over uncoded PAM-5 while the parity code achieves 3dB of coding gain. While encoding, the choice between encoders can be encoded in a TX_CODING bit, which can be set to one for trellis coding. One skilled in the art will recognize that embodiments of the present invention are applicable to any error correction technique.

Page 11, amend the heading at line 1 as follows:

4-D Trellis ~~*4D Trellis*~~ *Encoding*

Page 11, amend the paragraph beginning at line 3 as follows:

Trellis encoding in a conventional 4-D eight state code is described in Part II, Table IV of G. Ungerboeck, "Ungerboeck-Coded Modulation with Redundant Signal Sets, Part I and II", *IEEE Communications*, vol. 24, no. 2, pp. 5-21 (Feb., 1987) (hereinafter "Ungerboeck"). ~~Ungerboech").~~ An embodiment of an eight state trellis encoder 200 similar to that described in Ungerboeck is shown in Figure 2. Trellis encoder 200 receives eight bits, bits 0 through 7, and outputs 9 bits, bits 0 through 7 plus a parity bit, provided that TX_CODING is set to 1. The parity bit is produced from a rate 2/3 memory 3, systematic convolutional encoder 201.

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Page 11, amend the paragraph beginning at line 35 as follows:

Each 1-D PAM-5 symbol is a member of one of two families, X (odd) and Y (even). The odd set X contains the PAM-5 symbols {-1, +1} and the even set Y contains the PAM-5

symbols {-2, 0, +2}. Table 1 shows a definition of the eight subsets of 4-D symbols labeled D0 ~~DØ~~ through D7. The definition is based on the membership of 1-D PAM-5 symbols that are represented in each subset. Table 1 also shows the number of 4-D symbols included in each of the subsets.

Page 13, amend the paragraph beginning at line 8 as follows:

A point within subset p is chosen by the six least significant bits of the input, bits 0 through 5. Bits 0 through 5 are input to a 4-D PAM-5 mapper 211 along with the output of set select 210, χ. 4-D PAM-5 mapper 211 determines the 4-D PAM-5 symbol within set D_p which represents the eight input bits, bits 0 through 7, and the parity bit. Each subset, D0 ~~DØ~~ through D7, contains more than the 64 points required to encode the six bits, bits 0 through 5. These additional points are either used as control characters or not used at all.

Page 14, amend the paragraph beginning at line 3 as follows:

Figure 3 shows a trellis diagram resulting from the convolutional encoder shown in Figure 2. The states of the trellis in Figure 3, S_0 through S_7, are determined by the bits in delay elements 202, 204 and 206. The state S_q is determined by q=4*(the output signal from delay 202)+2*(the output signal from delay 204) + 1*(the output bit from delay 206). The subsets D_p are determined by the transition from one state to another as shown in Figure 3. The subsets ~~subsepts~~ D_p are given in Table 1.

Page 14, amend the paragraph beginning at line 13 as follows:

As shown in Figure 3, all transitions out of a particular state are either all even subsets ~~substates~~ (D_0, D_2, D_4, and D_6) or all odd subsets (D_1, D_3, D_5, and D_7). Similarly, the transitions into a particular state are either all even subsets or all odd subsets. The minimum squared distance between outgoing transitions, therefore, is equal to two (2) and the minimum squared distance between incoming transitions is also two (2).

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Page 14, amend the paragraph beginning at line 21 as follows:

As a result, the minimum squared distance between valid sequences is greater than or equal to 4, which can be seen from the fact that any two paths that originate from the same

node and end at the same node, but diverge at some point in the middle, must then converge at a later time. Both the divergence and the convergence have a squared distance of at least 2, thus the total squared distance must be at least 4. In the case where these two paths do not diverge, then they must contain different points from the same subset. Because the minimum squared distance between points in the same subset is equal to 4, the minimum squared distance between valid sequences is 4. As is conventionally known, ~~therefore,~~ a coding gain of 6dB with respect to uncoded PAM-5 constellations is therefore ~~are~~ experienced.

Page 15, amend the heading at line 3 as follows:

4-D Parity Code ~~*4D Parity code*~~

Page 16, amend the paragraph beginning at line 1 as follows:

An input symbol stream $\{a_{k,1}\}$ through $\{a_{k,N}\}$ is input to each of wires 103-1 through 103-N, respectively, of transmission channel 104 (Figure 1) by transmitter 101. Wires 103-1 through 103-N can be twisted copper pair, or some other transmission medium such as coaxial cable or optical fiber. Transmission channel 104 represents the effects that wires 103-1 through 103-N, transmission coupler 112 and receiver couplers in detector 108 have on the input symbol streams $\{a_{k,1}\}$ through $\{a_{k,N}\}$ in ~~$\{a_{k,N}\}$ in~~ transmission between transmitter 101 and receiver 107. Each transmission channel 104-1 through 104-N includes a corresponding one of wires 103-1 through 103-N, respectively, for the symbol stream $\{a_{k,1}\}$ through $\{a_{k,N},\}$ respectively.

Page 16, amend the paragraph beginning at line 27 as follows:

The channel response 105-L is represented by the channel function $f_L(Z)$. ~~$f_L(z)$.~~ In Figure 1, each of conductors 103-1 through 103-N can experience a different channel function $f_1(Z)$ through $f_N(Z)$, respectively. The addition of random noise $n_{k,L}$ in Figure 4 is represented by adder 106-L. Again, in Figure 1 each of conductors 103-1 through 103-N experiences a different random noise $n_{k,1}$ through $n_{k,N}$, respectively. The signal ~~signal,~~ $x_{k,L}$ suffering from channel distortion, random noise, and a flat signal loss ~~loss,~~ is received by receiver ~~by a receiver~~ 107.

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Page 17, amend the paragraph beginning at line 1 as follows:

For the sake of simplicity, a baseband transmission system is assumed, although the techniques shown are easily extended to a passband transmission system. (*See* E.A. LEE AND D.G. MESSERCHMITT, DIGITAL COMMUNICATIONS (1988)) It is also assumed that the channel model includes the effects of transmit and receive filtering. In addition, the transmission channel is assumed to be linear in that two overlapping signals simply add as a linear superposition. The Z-transform ~~Z-transform,~~ (*see* A. V. OPPENHEIM & R. W. SCHAFER, DISCRETE-TIME SIGNAL PROCESSING (1989)) ~~(1989)),~~ of the sampled transmission channel 104-L shown in Figure 4 is given by the channel function polynomial

$$f_L(Z)=f_{0,L} + f_{1,L}Z^{-1} + \ldots f_{j,L}Z^{-j} + \ldots + f_{R,L}Z^{-R}, \qquad (2)$$

where $f_{0,L}$, ..., $f_{j,L}$, ..., $f_{R,L}$ are the polynomial coefficients. The coefficient $f_{j,L}$ represents the dispersed component of the (k-j)th symbol present in the $a_{k,L}$th symbol and R is a cut-off integer such that $f_{j,L}$ for j>R is negligible. The polynomial $f_L(Z)$ represents the Z-transformation of the frequency response of the transmission channel (Z^{-1} represents a one period delay). (*See* A. V. OPPENHEIM & R. W. SCHAFER, DISCRETE-TIME SIGNAL PROCESSING (1989).) ~~(1989)).~~

Page 17, amend the paragraph beginning at line 26 as follows:

The noiseless output of the channel at sample time k is given by

$$r_{k,L} = f_{0,L} * a_{k,L} + f_{1,L} * a_{k-1,L} + \ldots f_{R,L} * a_{k-R,L}, \qquad (3)$$

where, without loss of generality, $f_{0,L}$ can be assumed to be 1. Thus, the channel output signal at time k depends, not only on transmitted data at time k, but on R past values of the transmitted data. This effect is known as "intersymbol interference" (ISI). (*See* LEE & MESSERSCHMITT.) ~~MESSERSCHMITT).~~ The ISI length of the transmission channel defined by Equations 2 and 3 is R, the number of past symbols contributing to ISI.

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Page 18, amend the paragraph beginning at line 24 as follows:

Figure 5A shows a ~~shows in a~~ block diagram of an embodiment of a baseband receiver system 500 according to the present invention. Other receiver systems may also utilize aspects of the present invention. Embodiments of receiver system 500 may include

any number of transport wires 103-1 through 103-N (with associated transmission channels 104-1 through 104-N, respectively) carrying input signal streams $x_{k,1}$ through $x_{k,N}$, respectively.

Page 18, amend the paragraph beginning at line 33 as follows:

Receiver system 500 includes receivers 501-1 through 501-N, one for each of lines 103-1 through 103-N, respectively. Receiver 501-j, an arbitrarily chosen one of receivers 501-1 through 501-N, includes filter/digitizer 502-j, equalizer 505-j, and coefficient update 506-j. Signal $x_{k,j}$ from wire 103-j is received by filter/digitizer 502-j. ~~Signals from wire 103-j, $x_{k,j}$, are received by filter digitizer 502-j.~~ Filter/digitizer 502-j filters, digitizes and amplifies the signal $x_{k,j}$ and outputs a signal $y_{k,j}$. Equalizer 505-j receives the signal $y_{k,j}$, equalizes it to remove the effects of intersymbol interference, and outputs a signal $a_{k,j}$, which is the output signal for receiver 501-j. Filter/digitizer ~~Filter/Digitizer~~ 502-j can be arranged to include filters that partially remove the ISI interference from signal $x_{k,j}$ before digitizing the signal. See, e.g., U.S. Patent Application 09/561,086, Monickam et al., ~~(See, e.g., Application Serial No. [Attorney Docket No. M-5789],~~ filed on the same date as the present application, ~~and~~ assigned to the same assignee as ~~as is~~ the present application, herein incorporated by reference in its entirety. ~~entirety).~~

Page 19, amend the paragraph beginning at line 17 as follows:

Coefficient update 506-j inputs decided-on ~~decided on~~ symbols $\hat{a}_{k,j}$ and other parameters and adaptively chooses parameters for filter/digitizer 502-j and equalizer 505-j (e.g., amplifier gain, multiplier coefficients, filter parameters, echo cancellation, NEXT cancellation, and timing parameters).

Page 19, amend the paragraph beginning at line 23 as follows:

One skilled in the art will recognize that each of receivers 501-1 through 501-N can be different. That is, ~~different(i.e.,~~ each of filter/digitizers ~~filters~~ 502-1 through 502-N and equalizers 505-1 through 505-N can be individually matched to receive input signals from the corresponding one of wires 103-1 through 103-N.

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Page 19, amend the paragraph beginning at line 29 as follows:

Figure 5B shows a representative example of receiver 501-j. Receiver 501-j is one of receivers 501-1 through 501-N. Receiver 501-j includes filter digitizer (or receiver/digitizer) ~~receiver/digitizer~~ 502-j in series with equalizer 505-j. Receiver/digitizer 502-j includes, in series, filter/echo ~~filters/echo~~ canceller ~~canceler~~ 508-j, analog-to-digital converter (ADC) 509-j, and amplifier 510-j. One skilled in the art will recognize that the order of these components can be altered from that shown in Fig. 5B. For example, amplifier 510-j can be implemented before ~~filter 502-j or~~ filter/echo canceller (or simply filter) 508-j, or filter 508-j can be implemented, completely or partially, digitally after ADC 509-j.

Page 20, amend the paragraph beginning at line 5 as follows:

Parameters to control the components of receiver 501-j ~~502-j~~ can be adaptively chosen by coefficient update 506-j. Coefficient update 506-j adaptively determines the equalizer coefficients of equalizer ~~equalizers~~ 505-j, the gain g_j of amplifier 510-j, the timing coefficient τ_j of ADC 509-j, and filter coefficients for filter 508-j. In some embodiments, coefficient update 506-j can calculate a baseline wander correction signal w_j ~~signal wj,~~ which is subtracted from the output sample of ADC 509-j at baseline wander correction adder 511-j. Baseline wander correction is discussed in ~~"Digital Baseline Wander Correction Circuit,"~~ U.S. Patent Application ~~No.~~ 09/151,525, filed July 11, 1998, ~~Sreen A.~~ Raghavan, assigned to the same assignee as the present application, ~~disclosure,~~ now U.S. Patent 6,415,003, herein incorporated by reference in its entirety.

Page 20, amend the paragraph beginning at line 24 as follows:

Echo noise, which is a result of impedance mismatches in the duplex link causing some of the transmitted signal energy to be reflected back into a receiver, and near end crosstalk (NEXT) noise, which is caused by the interference from a transmitter, i.e., transmitter 110 (Figure 1), ~~(Figure 1)~~ physically located adjacent to receiver 107, can be canceled through adaptive algorithms in filter 508-j. The cancellation of echo noise and NEXT noise is nearly complete because receiver system 500 has access to the data transmitted by an adjacent transmitter (transmitter 110 in Figure 1). Coefficient update 506-j, therefore, may input parameters from a decoder/slicer, host 151 or other controller in order

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to adjust filter 508-j to cancel echo and NEXT noise. Note that, in Figure 1, transmitter 101 may also be adjacent to an accompanying receiver 111.

Page 21, amend the paragraph beginning at line 20 as follows:

Amplifier 510-j amplifies the samples received from wire 103-j through transmission channel 104-j in order to correct for signal loss during transmission. The gain g_j of amplifier 510-j ~~The gain of amplifier 510-j, g_j,~~ can be adaptively chosen by coefficient update 506-j in order to optimize the operation of receiver 501-j. One of ordinary skill in the art will recognize that digital amplifier 510-j can be located anywhere in receiver 501-j ~~502-j~~ between ADC 509-j and equalizer 505-j. In general, amplifier 510-j can also be an analog amplifier located anywhere between input channel 104-j and ADC 509-j.

Page 21, amend the paragraph beginning at line 31 as follows:

In some embodiments, coefficient update 506-j can also calculate the length and quality of wire 103-j. Cable length and quality determination is discussed in U.S. Patent Application ~~No.~~ 09/161,346, ~~"Cable Length and Quality Indicator",~~ filed September 25, 1998, ~~Sreen A.~~ Raghavan et al., ~~and Doug J. Easton,~~ assigned to the same assignee as the present application, ~~disclosure,~~ now U.S. Patent 6,438,163, herein incorporated by reference in its entirety.

Page 22, amend the paragraph beginning at line 3 as follows:

The output sample $y_{k,j}$ from receiver/digitizer 502-j ~~The output sample from receiver/digitizer 502-j, $y_{k,j}$,~~ is input to equalizer 505-j. Equalizer 505-j can be any kind of equalizer structure. Types of equalizer structures include linear equalizers, decision feedback equalizers, and sequence detection equalizers. Equalizers of these types for 100 or 1000 BASE-T Ethernet over category-5 wiring, 24 gauge twisted copper pair, are described in ~~"Improved Detection for Digital Communication Receivers,"~~ U.S. Patent Application ~~No.~~ 08/974,450, filed November 20, 1997, ~~Sreen A.~~ Raghavan, assigned to the same assignee as the present application, now U.S. Patent 6,038,269, herein incorporated by reference in its entirety; and ~~"Simplified Equalizer for Twisted Pair Channel,"~~ U.S. Patent Application ~~No.~~ 09/020,628, filed February 9, 1998, ~~Sreen A.~~ Raghavan, assigned to the same assignee as the

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present application, ~~disclosure,~~ now U.S. Patent 6,115,418, herein incorporated by reference in its entirety.

Page 22, amend the paragraph beginning at line 20 as follows:

Additionally, receivers of the type described above as receivers 501-1 through 501-N are further described in U.S. Patent Applications 09/151,525 and 09/161,346, both cited above. ~~Additionally, receivers of the type described above as receivers 501-1 through 501-N are further described in "Digital Baseline Wander Correction Circuit," U.S. Application No. 09/151,525, filed July 11, 1998, Sreen A. Raghavan; and U.S. Patent Application No. 09/161,346, "Cable Length and Quality Indicator", filed September 25, 1998, Sreen A. Raghavan and Doug J. Easton, both of which have already been incorporated by reference.~~

Page 22, amend the paragraph beginning at line 29 as follows:

In receiver system 500 of Figure 5A, the output samples $a'_{k,1}$ through $a'_{k,N}$ from receivers 501-1 through 501-N, respectively, ~~the output samples from each of receivers 501-1 through 501-N, $a'_{k,1}$ through $a'_{k,N}$,~~ are input to decoder 507. Decoder 507 decides on a N-D symbol based on the samples from ~~each of~~ receivers 501-1 through 501-N. Each of the N 1-D symbols of the N-D symbol is the result of the N-D symbol pick in decoder 507.

Page 23, amend the paragraph beginning at line 1 as follows:

Figure 6 shows a block diagram of a linear equalizer 600 having R+1 multipliers, where R is any integer greater than or equal to 0. Linear equalizer 600 includes delays 601-1 through 601-R connected in series. The output samples from ~~each of~~ delays 601-1 through 601-R are ~~is~~ also input to multipliers 602-1 through 602-R, respectively. The input sample y_k to equalizer 600 is input to multiplier 602-0. The input samples to multipliers 602-0 through 602-R are multiplied by the corresponding one of multiplier coefficients C_0 through C_R, respectively, and summed in adder 603. Multiplier coefficients C_0 through C_R can be adaptively chosen to optimize the performance of equalizer 600. In Figure 5B, for example, coefficient update 506-j adaptively chooses equalizer parameters for equalizer 505-j.

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Page 23, amend the paragraph beginning at line 17 as follows:

Equalizer 600 (Figure 6) executes the transfer function

$$T = C_o + C_1 Z^{-1} + \cdots + C_j Z^{-j} + \cdots + C_R Z^{-R}. \qquad (6)$$

For simplicity, the wire designation L has been neglected. It is understood that each transmission channel includes a separated equalizer, each of which can be a unit ~~one~~ of equalizer 600 having its own transfer function T.

Page 23, amend the paragraph beginning at line 25 to read:

In a zero-forcing linear equalizer (ZFLE), the transfer function T is the inverse of the frequency response of the channel f(Z) (see Equation 2 with the wire designation L neglected). In a minimum mean squared error based linear equalizer (MMSE-LE), the transfer function is arranged to optimize the mean squared error between the transmitted data signal and the detected data symbols. A compromise, then, is found between the un-canceled ISI and the noise variance at the output terminal of the equalizer. (*See* B. SKLAR, DIGITAL COMMUNICATIONS, FUNDAMENTALS AND APPLICATIONS (PTR Prentice Hall, Englewood Cliffs, NJ, 1988).) ~~1988)).~~

Page 24, amend the paragraph beginning at line 4 as follows:

The output sample from linear equalizer 600, executing transfer function T, is given by

$$a'_k = C_0 y_k + C_1 y_{k-1} + \cdots + C_j y_{k-j} + \cdots + C_R y_{k-R}, \qquad (7)$$

where C_0 through C_R are the equalizer coefficients, y_{k-j} is the input signal to equalizer 600 during the time period that is j periods before the kth period, and k represents the current time period.

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Page 24, amend the paragraph beginning at line 11 as follows:

The output sample a'_k from equalizer 600 ~~The output sample from equalizer 600, a'_k,~~ is usually input to a slicer 604 which decides, based on its input sample a'_k, what symbol $\hat{a}_k$

was transmitted during time period k. The symbol $\hat{a}_k$ is chosen from the symbol alphabet used for transferring data that is closest to input signal a'_k.

Page 24, amend the paragraph beginning at line 17 as follows:

A linear equalizer can be implemented using either parity coding or trellis coding systems. When linear equalization is used with parity coding, a separate linear equalizer is used on each transport wire. In Figure 5A, for example, each of equalizers 505-1 through 505-N can include a linear equalizer. ~~The output samples from each of equalizers 505-1 through 505-N is input to decoder 507, which chooses the most appropriate multi-dimensional (N-D) symbol~~

Page 25, amend the paragraph beginning at line 4 as follows:

The input samples to linear equalizers 600-1 through 600-4 <u>are</u> ~~, corresponding to~~ the output samples <u>$y_{k,1}$ through $y_{k,4}$</u> from <u>receivers/digitizers</u> ~~receiver/digitizer~~ 502-1 through 502-4 (Figure 5B), ~~which is given by $y_{k,1}$ through $y_{k,4}$ samples,~~ respectively. The subscripts 1-4 reference each of the four wires 103-1 through 103-4, respectively. The output samples <u>$a'_{k,1}$ through $a'_{k,4}$</u> from linear equalizers 600-1 through <u>600-4</u>, ~~600-4 are given by $a'_{k,1}$ through $a'_{k,4}$~~, respectively, ~~and~~ are input to slicers 604-1 through 604-4, respectively. In Figure 7, slicers 604-1 through 604-4 are 1-D slicers. If PAM-5 symbol coding is utilized, then slicers 604-1 through 604-4 are 1-D PAM-5 slicers that each output the PAM-5 symbol closest to input sample $a'_{k,1}$ through $a'_{k,4}$, respectively.

Page 25, amend the paragraph beginning at line 18 as follows:

The output symbols <u>$\hat{a}_{k,1}$ through $\hat{a}_{k,4}$</u> from slicers 604-1 through 604-4, ~~$\hat{a}_{k,1}$ through $\hat{a}_{k,4}$~~, respectively, are input to parity check 702. Additionally, each of samples $a'_{k,1}$ through $a'_{k,4}$ is subtracted from the corresponding one of symbols $\hat{a}_{k,1}$ through $\hat{a}_{k,4}$, respectively, in adders 701-1 through 701-4, respectively, to calculate errors $e_{k,1}$ through $e_{k,4}$, respectively. In general~~, then,~~ the error signal $e_{k,i}$, where i is 1 through 4, is <u>then</u> given by

$$e_{k,i}=a'_{k,i}-\hat{a}_{k,i}\ . \qquad (8)$$

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Page 25, amend the paragraph beginning at line 27 as follows:

The parity of the 4-D symbol that results from the four 1-D symbols ~~four 1D symbols~~ is checked in parity check 702. In parity coding, the 4-D symbol ~~the 4D symbol~~ is chosen from an even subset of all 4-D symbols. Therefore, if PAM-5 coding is used, there are an even number of PAM-5 symbols from family X (odd symbols) and an even number from family Y (even symbols). Parity check 702 checks the parity of the four input symbols, $\hat{a}_{k,1}$ through $\hat{a}_{k,4}$, by determining whether the sum of the four symbols is even or not. An odd parity indicates that there is an error in at least one of the decided symbols $\hat{a}_{k,1}$ through $\hat{a}_{k,4}$. The result of the parity check is input to final decoder 704.

Page 26, amend the paragraph beginning at line 6 as follows:

The calculated error signals $e_{k,1}$ through $e_{k,4}$ are input to error analysis 703. Error analysis 703 determines which of the four error signals $e_{k,1}$ through $e_{k,4}$ is greatest and the sign of that error. Error analysis 703 outputs a sign signal Sgn ~~(sgn)~~ and an identifier W for the symbol having the greatest error. ~~error (W).~~

Page 26, amend the paragraph beginning at line 13 as follows:

Final decoder 704 inputs the parity signal from parity check 702, the four 1-D PAM-5 symbols $\hat{a}_{k,1}$ through $\hat{a}_{k,4}$ from slicers 604-1 through 604-4, ~~$\hat{a}_{k,1}$ through $\hat{a}_{k,4}$~~, respectively, the identifier W for the symbol having the greatest error~~, W,~~ and the sign Sgn of that error~~, sgn,~~ and outputs the PAM-5 symbols $\hat{a}'_{k,1}$ through $\hat{a}'_{k,4}$ in response. If the parity is even, ~~then~~ the 4-D symbol defined by 1-D symbols $\hat{a}'_{k,1}$ through $\hat{a}'_{k,4}$ is then given by $\hat{a}_{k,1}$ through $\hat{a}_{k,4}$, respectively. The parity coding scheme, therefore, will pass erroneous 4-D symbols ~~erroneous 4D symbols~~ containing simultaneous errors in two of the 1-D symbols.

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Page 26, amend the paragraph beginning at line 24 as follows:

If the parity is odd, however, the results of error analysis 703 are used to correct the output symbols. Because the symbol having the greatest error is the one that is most likely incorrect, the value of the symbol indicated by identifier W is corrected by either increasing or decreasing that symbol by one symbol in the symbol alphabet in response to the sign Sgn of the error (in this example, increased for a positive sign and decreased for a negative sign).

The new set of four symbols, the three uncorrected symbols having the lowest error and the corrected symbol, is output as the 4-D symbol defined by 1-D symbols $\hat{a}'_{k,1}$ through $\hat{a}'_{k,4}$.

Page 27, amend the paragraph beginning at line 1 as follows:

Although simple to implement, the primary disadvantage of a linear equalizer is that, while removing the ISI from the input signal, it may cause the random noise to be enhanced. This is especially true in twisted copper pair channels where the frequency response of the channel has significant attenuation across the transmitted signal bandwidth. Hence, in twisted-pair channels, such as is used with Gigabit Ethernet, ~~gigabit ethernet,~~ linear equalization often does not perform well enough to be practical.

Page 27, amend the paragraph beginning at line 11 as follows:

Figure 8 shows a decision feedback equalizer 800. Decision feedback equalizer 800 includes a feedforward ~~feed-forward~~ section 810, a feedback section 811 and an adder 804. Feedforward section 810 includes delays 801-1 through 801-M coupled in series, multipliers 802-1 through 802-M coupled to receive the output signals from delays 801-1 through 801-M, respectively, multiplier 802-0 coupled to receive the input sample to decision feedback equalizer 800, and an adder 803 coupled to receive the output signals from each of multipliers 802-0 through 802-M. The output signal from each of multipliers 802-0 through 802-M is the input signal to that multiplier multiplied by the corresponding one of feedforward ~~feed-forward~~ multiplier coefficients C_0 through C_M. Feedforward ~~feed-forward~~ multiplier coefficients C_0 through C_M can be adaptively chosen in order to optimize the performance of the equalizer. In Figure 5B, for example, coefficient update 506-j adaptively chooses equalizer coefficients to optimize the performance of receiver 501-j.

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Page 28, amend the subparagraph beginning at line 11 as follows:

One embodiment of feedback section 811 includes delays 805-1 through 805-P coupled in series. Multipliers 806-1 through 806-P are coupled to receive the corresponding output signals from delays 805-1 through 805-P, respectively. Multipliers 806-1 through 806-P multiply each of their input signals by the corresponding one of feedback multiplier coefficients B_1 through B_P, respectively. Feedback coefficients B_1 through B_P also can be

adaptively chosen. Adder 807 sums the output signals from each of multipliers 806-1 through 806-P. Feedback section 811, therefore, executes the transfer function

$$T_{FB} = B_1 Z^{-1} + B_2 Z^{-2} + \cdots + B_P Z^{-P}. \qquad (11)$$

The ~~Because the~~ input signal to feedback section 811 is symbol $\hat{a}_k$. Consequently, the output signal from feedback section 811 is given by

$$a_k'' = B_1 \hat{a}_{k-1} + B_2 \hat{a}_{k-2} + \cdots + B_N \hat{a}_{k-P}. \qquad (12)$$

Page 29, amend the paragraph beginning at line 5 as follows:

The output signal a_k'' from feedback section 811~~, a_k'',~~ is subtracted from the output signal a_k' from feedforward section 810~~, a_k',~~ in adder 804. The input signal to slicer 808, then, is given by

$$a_k''' = a_k' - a_k''. \qquad (13)$$

Slicer 808 outputs the symbol $\hat{a}_k$ that is closest to the input signal a_k'''.

Page 29, amend the paragraph beginning at line 12 as follows:

A decision feedback equalizer operates on the principle that if the past transmitted data is correctly detected, ~~then~~ the ISI effects of these past data symbols can then be canceled from the currently received sample. As such, ~~often~~ feedforward section 810 often contains no multipliers (i.e., $C_0 = 1$ and all other coefficients are 0) and output sample a_k' equals ~~$= y_k$,~~ ~~the~~ input sample y_k.

Page 29, amend the paragraph beginning at line 26 as follows:

Figure 9 shows the equalization and decoder sections (*see* equalizers ~~Equalizers~~ 505-1 through 505-4 and decoder 507 of Figure 5, for example) of a 4-D receiver ~~a 4D receiver~~ 910. The equalization is accomplished using four decision feedback equalizers, one for each of the four input channels shown. Again, one skilled in the art will recognize that a receiver can have any number of input channels and that a 4-D receiver is shown here for example only. In Figure 9, receiver 910 includes 4-D decoder 900. Although decoder 900 is shown as a parity ~~Parity~~ code decoder, it is understood that decoder 900 can be any 4-D decoder.

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One skilled in the art will recognize that 4-D decoder 900 must correct symbols within a single clock cycle so that the results can be fed back through feedback sections (or taps) ~~FB taps~~ 811-1 through 811-4 to correct symbols $a'_{k,1}$ through $a'_{k,4}$, respectively.

Page 30, amend the paragraph beginning at line 9 as follows:

The equalization for channel 104-1, for example, is accomplished by feedforward section (or tap) 810-1, feedback section 811-1, and adder 804-1. Similarly, channels 104-2 through 104-4, each includes the corresponding ones of feedforward sections (or taps) ~~taps~~ 810-2 through 810-4, respectively, feedback sections 811-2 through 811-4, respectively, and adders 804-2 through 804-4, respectively.

Page 30, amend the paragraph beginning at line 17 as follows:

Samples $y_{k,1}$ through $y_{k,4}$ originate from receiver input signals received from channels 104-1 through 104-4, respectively. Samples $y_{k,1}$ through $y_{k,4}$ are received into feedforward taps 810-1 through 810-4, respectively. The symbol outputs $\hat{a}'_{k,1}$ through $\hat{a}'_{k,4}$ from decoder 900, ~~$\hat{a}'_{k,1}$ through $\hat{a}'_{k,4}$~~, corresponding to a single 4-D symbol, are input to feedback taps 811-1 through 811-4, respectively. As was discussed with relation to Figure 8, the output signal ~~signals~~ $a''_{k,1}$ through $a''_{k,4}$ from each of feedback sections 811-1 through 811-4, ~~$a''_{k,1}$ through $a''_{k,4}$~~, respectively, is subtracted from the corresponding one of the output signals $a'_{k,1}$ through $a'_{k,4}$ from feedforward sections 810-1 through 810-4, ~~$a'_{k,1}$ through $a'_{k,4}$~~, respectively, in each of adders 804-1 through 804-4, respectively. The output signals $a'''_{k,1}$ through $a'''_{k,4}$ from adders 804-1 through 804-4, ~~$a'''_{k,1}$ through $a'''_{k,4}$~~, respectively, are inputted to decoder 900.

Page 30, amend the paragraph beginning at line 33 as follows:

In an embodiment where decoder 900 is a 4-D parity code decoder, the input signals $a'''_{k,1}$ through $a'''_{k,4}$ to decoder 900 ~~900, $a'''_{k,1}$ through $a'''_{k,4}$~~ are received by slicers 901-1 through 901-4, respectively. Each of slicers 901-1 through 901-4 decides on an output symbol ~~symbol,~~ $\hat{a}_{k,1}$ through $\hat{a}_{k,4}$, respectively, based on its corresponding input signal ~~signal,~~ $a'''_{k,1}$ through $a'''_{k,4}$, respectively. The output symbols from slicers 901-1 through 901-4 are inputted to parity check 903 and final decoder 905.

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Page 31, amend the paragraph beginning at line 6 as follows:

Parity check 903 sums the 1-D symbols ~~the 1D symbols~~ $\hat{a}_{k,1}$ through $\hat{a}_{k,4}$ and determines whether the 4-D symbol ~~the 4D symbol~~ is of even parity or odd parity. In parity coding using PAM-5 symbols, the 4-D symbol ~~the 4D symbol~~ is chosen from an even subset and therefore each 4-D symbol ~~each 4D symbol~~ includes an even number of 1-D PAM-5 symbols from family X (odd parity) and an even number from family Y (even parity). Therefore, the sum of the 1-D PAM-5 symbols is even. If the parity of the 4-D symbol is even, ~~then~~ final decoder 905 then outputs the symbols $\hat{a}_{k,1}$ through $\hat{a}_{k,4}$ as output symbols $\hat{a}'_{k,1}$ through $\hat{a}'_{k,4M}$, respectively.

Page 31, amend the paragraph beginning at line 17 as follows:

Error signals $e_{k,1}$ through $e_{k,4}$ are calculated in adders 902-1 through 902-4, respectively, by, in each of the transport channels, taking the difference between the output symbol $\hat{a}_{k,1}$ through $\hat{a}_{k,4}$ of slicers 901-1 through 901-4, ~~$\hat{a}_{k,1}$ through $\hat{a}_{k,4}$~~, respectively, and the corresponding one of the input signal ~~signals~~, $a'''_{k,1}$ through $a'''_{k,4}$, respectively:

$$e_{k,i}=a'''_{k,i}-\hat{a}_{k,i}\text{, i=1, 2, 3 or 4.} \qquad (14)$$

The error signals $e_{k,1}$ through $3_{k,4}$ at each of slicers 901-1 through 901-4, respectively, are input to error analysis 904. Error analysis 904 determines which of the symbols $\hat{a}_{k,1}$ through $\hat{a}_{k,4}$ is associated with the largest error signal $e_{k,1}$ through $e_{k,4}$, respectively, and the sign of the largest error. Error analysis 904 outputs an identifier W of the symbol having the largest absolute error~~, W,~~ and the sign SGN of that error~~, SGN,~~ to final decoder 905. If the parity signal indicates odd parity, the erroneous symbol is most likely to be the one with the largest error, indicated by identifier W. Final decoder 905, then, adjusts the symbol having the largest error up or down the symbol alphabet by one symbol depending on the sign SGN (in this example, up if the sign is positive and down if the sign is negative) and outputs the resulting 4-D output symbol defined by $\hat{a}'_{k,1}$ through $\hat{a}'_{k,4}$.

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Page 33, amend the paragraph beginning at line 14 as follows:

The output samples $\hat{a}_{k,1}$ through $\hat{a}_{k,4}$ from sequence detectors 1001-1 through 1001-4, ~~$\hat{a}_{k,1}$ through $\hat{a}_{k,4}$~~, respectively, along with the second best output samples ~~samples~~, $\hat{a}2_{k,1}$

through $\hat{a}2_{k,4}$ and ~~, and~~ the errors Δ_1 through Δ_4 are input to decoder 1002. Decoder 1002 decides on the receiver output samples ~~samples,~~ $\hat{a}'_{k,1}$ through $\hat{a}'_{k,4}$ based ~~, based~~ on, for example, the parity coding scheme or the N-D lattice coding scheme. One skilled in the art will recognize that the decision of decoder 1002 can be based on any coding scheme that can correct errors in one clock cycle. Feedback is provided to sequence detectors 1001-1 through 1001-4 so that future sequences are decided using the results of the N-D decisions.

Page 33, amend the paragraph beginning at line 27 as follows:

Figure 11A shows a block diagram of a sequence detector 1100 for the PAM-5 symbol alphabet, {A}={+2, +1, 0, -1, -2}, where the intersymbol interference includes the effects of only one other symbol, i.e., the ISI length δ is one (1). In general, sequence detector 1100 can utilize any alphabet and any number of ISI symbols (A>2 and δ>1). Detector 1100 includes a branch metric generator ~~Branch Metric Generator~~ 1101, an add-compare-select ~~Add-Compare-Select~~ (ACS) unit 1102, traceback circuitry ~~Traceback Circuitry~~ 1103, a last-in-first-out ~~Last In First Out~~ (LIFO) buffer 1104, and a starting point determiner 1105. Sequence detectors are discussed in U.S. Patent Application ~~No.~~ 08/974,459, cited above. ~~, "Detection for Digital Communication Receivers," to Sreen Raghavan, which has been previously incorporated by reference in this application.~~

Page 34, amend the paragraph beginning at line 6 as follows:

The ISI addressed by the embodiment of detector 1100 shown in Figure 11A ~~Figure 11~~ is caused by just one previously transmitted symbol. Thus, the input sample to sequence detector ~~detectors~~ 1100 is given by

$$r_{k,w} = a_{k,w} + \alpha_1 a_{k-1,w} + h_{k,w} \quad , \qquad (15)$$

where ~~where,~~ $\alpha_{1,w}$ is the equalizer ISI coefficient, $h_{k,w}$ is the noise component of the output signal from the linear filter over a wire ~~over wire~~ w and $a_{k,w}$ is the transmitted symbol over wire w received in time period k. The sequence detector estimates the transmitted data sequence $\{a_{k,w}\}$ from the sequence of received samples $\{r_{k,w}\}$.

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Page 34, amend the paragraph beginning at line 17 as follows:

The state $S_{k,w}$ of detector 1100 ~~The state of detector 1100, $S_{k,w}$,~~ is defined as the past data symbol estimates. In general, a system with a symbol alphabet having A symbols and which suffers intersymbol interference from δ previous symbols will have A^{δ} possible states. Each state corresponds to a possible transition path through the δ previous symbols. For example, a system using a symbol alphabet with two symbols, {A} = {+1, -1}, and suffering ISI from two past symbols, δ=2, will have four possible sequence states of the system: symbol +1 at time k-2 and symbol +1 at time k-1; symbol +1 at time k-2 and symbol -1 at time k-1; symbol -1 at time k-2 and symbol +1 at time k-1; and symbol -1 at time k-2 and symbol -1 at time k-1. Sequence detector 1100 for the example embodiment shown in Figure 11A, a PAM-5 symbol alphabet with ISI resulting from one symbol, has five states -- +2, +1, 0, -1, and -2 -- corresponding to the five symbols in the PAM-5 alphabet {A}.

Page 35, amend the paragraph beginning at line 13 as follows:

In sequence detector 1100 shown in Figure 11A, branch ~~a branch~~ metric generator 1101 generates distance metrics corresponding to the branches illustrated in the trellis diagram of Figure 12. The distance metrics represent the difference between the input signal $r_{k,w}$ to branch metric generator 1101 ~~1101, $r_{k,w}$,~~ and the calculated signal that is expected to be observed in each of the allowed transitions of a trellis diagram. In general, if there are A^{δ} states of sequence detector 1100, ~~1100 then~~ there are $A^{\delta+1}$ branch metrics to calculate. In some embodiments, however, not all branches are allowed and therefore the number of branch metrics is reduced.

Page 35, amend the paragraph beginning at line 25 as follows:

For PAM-5 signaling suffering from one ISI symbol, there are twenty five (25) distance metrics $M_{k,w}$. The twenty five (25) distance metrics generated by branch metric generator 1101 for the case where ISI is the result of one past symbol and neglecting random noise (i.e., ~~i.e.~~ A=5, δ=1 and $f_w(z) = 1+\alpha_{w,1}z^{-1}$) are given by:

$M_{k,w}(0)=[r_{k,w}-(-2-2\alpha_{w,1})]^2$; $M_{k,w}(13)=[r_{k,w}-(\alpha_{w,1})]^2$;
$M_{k,w}(1)=[r_{k,w}-(-2-\alpha_{w,1})]^2$; $M_{k,w}(14)=[r_{k,w}-(2\alpha_{w,1})]^2$;
$M_{k,w}(2)=[r_{k,w}-(-2)]^2$; $M_{k,w}(15)=[r_{k,w}-(1-2\alpha_{w,1})]^2$;

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$M_{k,w}(3)=[r_{k,w}-(-2+\alpha_{w,1})]^2$; $M_{k,w}(16)=[r_{k,w}-(1-\alpha_{w,1})]^2$;
$M_{k,w}(4)=[r_{k,w}-(-2+2\alpha_{w,1})]^2$; $M_{k,w}(17)=[r_{k,w}-1]^2$;
$M_{k,w}(5)=[r_{k,w}-(-1-2\alpha_{w,1})]^2$; $M_{k,w}(18)=[r_{k,w}-(1+\alpha_{w,1})]^2$;
$M_{k,w}(6)=[r_{k,w}-(-1-\alpha_{w,1})]^2$; $M_{k,w}(19)=[r_{k,w}-(1+2\alpha_{w,1})]^2$;
$M_{k,w}(7)=[r_{k,w}-(-1)]^2$; $M_{k,w}(20)=[r_{k,w}-(2-2\alpha_{w,1})]^2$;
$M_{k,w}(8)=[r_{k,w}-(-1+\alpha_{w,1})]^2$; $M_{k,w}(21)=[r_{k,w}-(2-\alpha_{w,1})]^2$;
$M_{k,w}(9)=[r_{k,w}-(-1+2\alpha_{w,1})]^2$; $M_{k,w}(22)=[r_{k,w}-2]^2$;
$M_{k,w}(10)=[r_{k,w}-(-2\alpha_{w,1})]^2$; $M_{k,w}(23)=[r_{k,w}-(2+\alpha_{w,1})]^2$;
$M_{k,w}(11)=[r_{k,w}-(-\alpha_{w,1})]^2$; $M_{k,w}(24)=[r_{k,w}-(2+2\alpha_{w,1})]^2$;
$M_{k,w}(12)=[r_{k,w}]^2$. (16)

Page 36, amend the paragraph beginning at line 10 as follows:

Other metrics which represent the difference between the input symbol and the predicted input symbols, assuming each of the possible state transitions, may be used as distance metrics. In general, there will be a distance metric for every transition from any state S' at time k-1 to state S at time k, $A^{\delta+1}$ distance metrics for a metrics system with A symbols and δ interfering symbols if all transitions are allowed. PAM-5 symboling is shown here only as an example and embodiments of detector 1100 can utilize other symbol alphabets and more ISI symbols.

Page 36, amend the paragraph beginning at line 21 as follows:

Add-compare-select ~~(ACS)~~ circuit 1102 in Figure 11A updates a state metric, denoted by $p_{k,w}(+2)$, $p_{k,w}(+1)$, $p_{k,w}(+0)$, $p_{k,w}(-1)$, and $p_{k,w}(-2)$ in the PAM-5 example, for each possible state of the system ~~system, denoted by $p_{k,w}(+2)$, $p_{k,w}(+1)$, $p_{k,w}(+0)$, $p_{k,w}(-1)$, and $p_{k,w}(-2)$ in the PAM-5 example,~~ at each time step k. For the PAM-5 symbol alphabet the state metrics are given by:

$p_{k,w}(i) = \min_{j=\{-2,-1,0,1,2\}}\{p_{k-1,w}(j) + M_{k,w}((j+2)+5(i+2)\}$;
for $i=\{2,1,0,-1,-2\}$. (17)

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Page 36, amend the paragraph beginning at line 31 as follows:

In general, the state metrics represent the accumulated distance metrics of past states along transition paths that minimize the accumulated distance metric. Therefore, the transition metric $p_{k,w}(S)$ for state S at time period k ~~period k, $p_{k,w}(S)$,~~ is the accumulated

distance metric for previous states along a transition path which ends at state S at time period k, state S being one of the possible states of the system. At time k-1, the state of the system may be at any state S' in the group of possible states of the system. Therefore, $p_{k,w}(S)$ is the minimum one of $p_{k-1,w}(S')$ plus the distance metric for transition from S' to S. A mathematical proof that this technique results in the least detection error is given in the Appendix of ~~"Improved Detection for Digital Communication Receivers,"~~ U.S. Patent Application ~~No.~~ 08/974,450, cited above.

Page 37, amend the paragraph beginning at line 11 as follows:

In the example of Figure 11A, the comparison results ~~results,~~ $D_{k,w}(+2)$, $D_{k,w}(+1)$, $D_{k,w}(0)$, $D_{k,w}(-1)$ and $D_{k,w}(-2)$ ~~$D_{k,w}(-2)$,~~ are stored in a memory of traceback circuit 1103 for each of the five states. The comparison results indicate the state at time period k-1 which results in the state metric $p_{k,w}(S)$ for state S at time period k. In the PAM-5, $\delta=1$ example shown in Figure 11A, the ACS results for each of the five states are given by

$$D_{k,w}(i)=j \text{ if } p_{k,w}(i) = p_{k-1,w}(j)+M_{k,w}((j+2)+5(i+2)); \quad \text{for } i=\{2,1,0,-1,-2\}; j=\{2,1,0,-1,-2\}. \tag{18}$$

In general, $D_{k,w}(S)$ points toward the state S' at time k-1 from which results the lowest state metric for arriving at state S at time k.

Page 38, amend the paragraph beginning at line 3 as follows:

During the traceback procedure, starting ~~a starting~~ state determiner 1105 picks the starting state, which can be based on the state metrics $P_{k,w}(S)$. ~~$P_{k,w}(s)$.~~ Traceback circuit 1103 ~~1105~~ follows the sequence back through the comparison results stored in memory in traceback circuit 1103. The earliest TB/2 symbols, which result in the earliest states, are written into last-in-first-out ~~(LIFO)~~ buffer 1104. The new comparison results are stored in the memory locations previously occupied by the outputted results.

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Page 38, amend the paragraph beginning at line 13 as follows:

Traceback circuit 1103 determines the optimum sequence of symbols based on the state metrics $P_{k,w}(S)$ stored ~~$P_{k,w}(s)$stored~~ in starting state determiner 1105. Starting state determiner 1105 initializes the traceback procedure by setting a starting sequence.

Page 38, amend the paragraph beginning at line 26 as follows:

When the channel ISI length δ is large, or if the transmitted symbol alphabet size A is large, the above method of full sequence estimation becomes impractical at high symbol rates. Full sequence estimations require the implementation of A^{δ} states in the detector. Accordingly, equalizer ~~an equalizer~~ 1110 can provide pre-equalization by preprocessing the input samples $y_{k,w}$ in order to reduce the number of ISI symbols to be processed by sequence detector 1100. Equalizer 1110 can be any equalizer that reduces the number of ISI symbols. Again, for purposes of example, assume that the channel input alphabet size is A=5, i.e., ~~i.e.~~ {A}={+2, +1, 0, -1, -2}, and that the reduced ISI length (as seen by the sequence detector) is $\delta'=1$. As before, the technique is applicable to larger alphabets and may accommodate more than one interfering symbol in the reduced length.

Page 39, amend the paragraph beginning at line 7 as follows:

The output of the equalizer 1110 with A=5 and $\delta'=1$ is, analogous to Equation 15, ~~as previously described,~~ given by

$$r_{k,w}=a_{k,w}+\alpha_{w,1}*a_{k-1,w}+h_{k,w}, \qquad (19)$$

where $\alpha_{w,1}$ is the equalized ISI coefficient and h_k is the noise component of the output of the linear equalizer 1110. The transfer function (in Z-transform notation, *see* ~~See~~ A. V. OPPENHEIM AND R.W. SCHAFER, DISCRETE-TIME SIGNAL PROCESSING, (1989)) for equalizer 1110 is then given ~~is, then, given~~ by

$$E_w(z)=(1+\alpha_{w,1}z^{-1})/f_w(z). \qquad (20)$$

The coefficient $\alpha_{w,1}$ is chosen to minimize the noise variance at the output of the equalizer. Equalizer 1110, therefore, is a reduced sequence equalizer because it reduces the ISI length from δ to δ'. The reduced ISI length δ' is one (1) in this example.

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Page 39, amend the paragraph beginning at line 25 as follows:

In one embodiment, reduced sequence equalizer 1110 is implemented adaptively. One architecture used for adaptive implementation is shown in Figure 11B. In this embodiment, equalizer 1110 includes a linear equalizer 1120 implementing a transfer function $C(Z) = 1/f(Z) = C_0 + C_1Z^{-1}$ ~~C_1Z^{-1}~~ $+ \ldots + C_{\delta}Z^{-\delta}$, adaptively followed by a filter 1121

implementing the function $(1+\alpha_{w,1}Z^{-1}$ ~~$1+\alpha_{w,1}z^{-1}$~~ $+ \ldots +\alpha_{w,\delta'}Z^{-\delta'})$. By implementing both equalizer 1120 and filter 1121 adaptively, optimal performance can be achieved for any cable length. Linear equalizer 1120 can be adaptively implemented by using the least mean squares (LMS) algorithm (*see* ~~*See*~~ E.A. LEE AND D.G. MESSERCHMITT, DIGITAL COMMUNICATIONS (1988)) and a finite impulse response filter as shown in Figure 6.

Page 40, amend the paragraph beginning at line 3 as follows:

The coefficients $\alpha_{w,1}$ through $\alpha_{w,\delta'}$ can be chosen adaptively in the sequence detector by observing the frequency response of linear equalizer 1120. From linear equalizer 1120, the channel frequency response is deduced and $\alpha_{w,1}$ through $\alpha_{w,\delta'}$ can be selected from a look-up table. In one embodiment with $\delta'=1$, two possible values of $\alpha_{w,1}$ (0 and 1/2) are used. One of the two possible coefficients is chosen for $\alpha_{w,1}$ by observing the two largest equalizer coefficients of linear equalizer 1120, C_0 and C_1. For example, in one embodiment, ~~embodiments~~ if $C_1/C_0 < -0.5$ then $\alpha_{w,1} = 0.5$, otherwise $\alpha_{w,1} = 0$.

Page 40, amend the paragraph beginning at line 20 as follows:

In the example described in connection with Figure 11B ~~11~~ with $\delta'=1$, the number of states in the sequence estimator is reduced from 5^{δ} to 5. The reduced state sequence estimator can be implemented using the Viterbi algorithm.

Page 40, amend the paragraph beginning at line 29 as follows:

Figure 13 shows a receiver 1350 that includes an embodiment of a sequence detector 1300 having decision-feedback. In this embodiment, equalizer 1301, which as before can be any equalizer structure, pre-equalizes transmission channel 104-w to a pre-determined ISI polynomial $G_w(z)$ of length $\eta \leq \delta$, where δ is the ISI length of the frequency response $f_w(z)$ of ~~response $f_w(Z)$ of~~ transmission channel 104-w. In one example, ~~the example of Figure 11,~~ η is 2 and the ISI polynomial $G_w(z)$ is given by

$$G_w(z) = 1 + \alpha_{w,1}z^{-1} + \alpha_{w,2}z^{-2}. \quad (21)$$

The transfer function of equalizer 1301 is given by

$$E_w(z) = G_w(z)/f_w(z). \quad (22)$$

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Page 41, amend the paragraph beginning at line 10 as follows:

Sequence detector 1300 includes branch metric generator 1302, add compare select (unit) 1303, traceback (circuit) 1304, LIFO 1305 and starting point determiner 1306. In general, the detection technique implemented in sequence estimator 1300 may be used for any combination of δ and η such that $\eta \leq \delta$. Although the technique may be implemented with any sized alphabet, the example shown in Figure 13 is for the PAM-5, (A=5), alphabet. The coefficients, $\alpha_{w,1}$ and $\alpha_{w,2}$, can be chosen adaptively to optimize performance of the receiver 1350.

Page 42, amend the paragraph beginning at line 30 as follows:

Add compare select ~~(ACS)~~ 1303 then computes the state metrics $p_{k,w}(j)$ and the comparison results $D_{k,w}(j)$ as described above in Equations 17 and 18, ~~equations 16 and 17,~~ respectively. Traceback 1304 accepts a starting point from starting point determiner 1306, as described above for the corresponding components of sequence detector 1100 in Figure 11A, and outputs a set of decided-on ~~decided on~~ symbols to LIFO 1305. LIFO 1305, then, outputs the resulting symbols in reverse chronological order from that received.

Page 43, amend the heading at line 4 as follows:

Sequence Detection ~~detection~~ in Combination ~~combination~~ with Error Correction ~~error correction~~

Page 43, amend the paragraph beginning at line 23 as follows:

Figure 14 shows a sequence detector 1400-w according to the present invention. Sequence detector 1400-w is coupled to receive signal $r_{k,w}$ from wire w. Sequence detector 1400-w includes branch metric generator 1402-w, add compare select (unit) ~~(ACS)~~ 1403-w, and starting point determiner 1406-w. Add compare select 1402-w and starting point determiner 1406-w are each coupled to traceback 1404.

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Page 44, amend the paragraph beginning at line 1 as follows:

A ~~Although a~~ sequence detector according to the present invention can accommodate any symbol alphabet and any number of ISI symbols. For example, ~~symbols, for example~~ sequence detector 1400 shown in Figure 14 is for a PAM-5 alphabet where input signals suffer the influence of one past ISI symbol (i.e., the ISI length is 1). As occurs with equalizer 1110 in Figure 11A (see Equation 20), equalizer 1401-w ~~Equalizer 1401-w, as has been previously discussed,~~ executes a transfer function $E(Z) = (1+\alpha_{w,1}Z^{-1})/f_w(Z)$ and therefore sequence detector 1400-w detects a signal that includes ISI from one past symbol. Branch metric generator 1402-w ~~1402-w,~~ therefore generates the branch metrics as described in Equation 16.

Page 44, amend the paragraph beginning at line 13 as follows:

Add compare select ~~(ACS)~~ 1403-w computes the state metrics $p_{k,w}(i)$ (i=-2,-1,0,1,2) according to Equation 17 and the ACS results $D_{k,w}(i)$ according to Equation 18. Additionally, ACS 1403-w computes a second best state metric $p2_{k,w}(i)$, a second ACS result $D2_{k,w}(i)$, and a difference result $\Delta_{k,w}(i)$. The second best state metric can be computed according to the equation

$p2_{k,w}(i)$= second minimum $(p_{k-1,w}(j) + M_{k,w}(5(i+2)+(j+2)))$;
j={-2, -1, 0, 1, 2}, (24)

where i={-2, -1, 0, 1 2}. The second ACS result can be computed according to

$$D2_{k,w}(i) = j \text{ if } p2_{k,w}(i) = p_{k-1,w}(j) + M_{k,w}(5(i+2)+(j+2)), \quad (25)$$

where i={-2,-1,0,1,2} and j=(-2,-1,0,1,2}. Finally, the difference result can be computed according to

$$\Delta_{k,w}(i) = p2_{k,w}(i) - p_{k,w}(i). \quad (26)$$

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Traceback 1404 receives the ACS results, the second ACS results, and the difference results from each state on each wire as well as a starting point signal from starting point determiner 1406-w for each wire w.

Page 45, amend the paragraph beginning at line 5 as follows:

Figure 15 shows an embodiment of ~~of a~~ 4-D traceback 1404 for use ~~in combination~~ with a series of sequence detectors 1400-w. For ~~It is understood that, in general, for~~ an N-wire configuration, traceback 1404 is generally coupled into N sequence detectors similar to that shown in Figure 14, one for each wire w. In Figure 15, traceback 1404 includes a parity code decoder 1504 although other coding schemes can be used, provided that the coding scheme can correct symbols within one clock cycle.

Page 45, amend the paragraph beginning at line 14 as follows:

For exemplary purposes, Figure 15 shows a four-wire parity-code decoder. Traceback 1404 includes read modules ~~a read module~~ 1501-1 through 1501-4, one for each of the four wires. Each read ~~Read~~ module 1501-1 through 1501-4 receives parameters $\Gamma_{k,w}$ from add compare select 1403-w and starting point determiner 1406-w (Figure 14). Parameters $\Gamma_{k,w}$ includes the add compare results $D_{k,w}(i)$, $D2_{k,w}(i)$ and $\Delta_{k,w}(i)$, where i=(-2, -1, 0, 1, 2) for PAM-5 signaling, as well as a starting point $SP_{k,w}$ for each wire w. As was discussed before, starting point determiner 1406-w chooses a starting point $SP_{k,w}$, which can be based on the state metrics $p_{k,w}(i)$, for traceback 1404.

Page 45, amend the paragraph beginning at line 32 as follows:

As described above, the 4-D parity coding scheme only transmits 4-D symbols having even parity. A single error in one 1-D symbol will cause the parity of the 4-D symbol to become odd. Similar to "4-D slicing", traceback 1404 recognizes the parity error and makes corrections to the four 1-D ~~to the 4-1-D~~ symbols from read modules 1501-1 through 1501-4 for clock cycle k based on the reliability of each of the 1-D symbols.

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Page 46, amend the paragraph beginning at line 4 as follows:

Hagenauer has shown that, within a Viterbi decoder, the reliability of decision symbol paths merging at each state grows with the difference between the state metrics between the two paths. *See* J. Hagenauer and P. Hocher, "A Viterbi Algorithm with Soft-Decision Outputs and its Applications," Proc. GLOBECOM '89, 1680-1686, November 1989. ~~1989).~~ Similar to Hageauer's Soft Output Viterbi Algorithm (SOVA), each of read modules 1501-1 through 1501-4 outputs the difference metric, i.e., ~~i.e.~~ the reliability measure, between the best two paths entering each state, $\varepsilon_{k,1}$ through $\varepsilon_{k,4}$, respectively. SOVA uses these metrics over a range of sample times within the trellis to output soft decisions for every symbol.

Page 46, amend the paragraph beginning at line 26 as follows:

For each clock cycle k, traceback 1404 retrieves each of the first choice 1-D symbols $\hat{a}_{k,1}$ through $\hat{a}_{k,4}$, the second choice 1-D symbols $\hat{a}2_{k,1}$ through $\hat{a}2_{k,4}$, and the reliability measures $\varepsilon_{k,1}$ through $\varepsilon_{k,4}$, and determines the finally decided four 1-D ~~decided 4 1-D~~ symbols $\hat{a}'_{k,1}$ through $\hat{a}'_{k,4}$.

Page 46, amend the paragraph beginning at line 31 as follows:

For each clock cycle k, parity check 1502 receives the first choice symbols $\hat{a}_{k,1}$ through $\hat{a}_{k,4}$ from read modules 1501-1 through 1501-4, respectively, determines the parity of the resulting 4-D symbol and outputs a parity signal indicating the parity of the 4-D symbol. Error analysis 1503 receives reliability measures $\varepsilon_{k,1}$ through $\varepsilon_{k,4}$ from read modules 1501-1 through 1501-4, respectively, determines which of the sequence detectors w has the least reliability, thereby indicating which result is most likely to be incorrect, and outputs a wire signal W indicating which symbol is most likely to be incorrect. Decoder 1504 receives the first choice symbols $\hat{a}_{k,1}$ through $\hat{a}_{k,4}$, the second choice symbols $\hat{a}2_{k,1}$ through $\hat{a}2_{k,4}$, the parity signal from parity check 1502, and the wire signal from error analysis 1503.

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Page 47, amend the paragraph beginning at line 32 as follows:

In other words, read module 1501-w outputs the best possible step back $\hat{a}_{k,w}$, the second best step back $\hat{a}2_{k,w}$, and the reliability measure $\varepsilon_{k,w}$ for each wire for clock cycle k. Parity check 1502 performs a parity check on the best possible step back $\hat{a}_{k,w}$. Error analysis

1503 determines the wire most likely to be incorrect. If the parity passes, decoder 1504 outputs the best possible step back $\hat{a}_{k,w}$ for clock cycle k. If parity fails, then decoder 1504 replaces one of the best possible symbols with the associated second best symbol, based on which wire is most likely to be incorrect, and outputs the resulting 4-D symbol. The choice of best symbol or second best symbol for each wire w is communicated back to read module 1501-w so that read module 1501-w can use the appropriate symbol to step back to clock cycle k-1. The replacement choice then ~~, then,~~ affects only one read module. Therefore, the next set of symbols will be affected in one read module only.

Page 48, amend the paragraph beginning at line 32 as follows:

If the alphabet size is large or if the ISI length at the sequence detector is large then sequence detector 1400-w shown in Figure 14 and traceback 1404 using parity coding shown in Figure 15 become impractical at high symbol rates. The number of states required in read modules 1501-1 through 1501-4 is A^{η} on each wire, where A represents the number of symbols in alphabet {A} and η represents the ISI symbol length at the sequence detector (i.e., ~~i.e.~~ at the input terminal of sequence detector 1400 in Figure 14). With a PAM-5 alphabet and η=2 ISI symbols, each of read modules 1501-1 through 1501-4 requires twenty five (25) states in order to perform sequence detection. A decoder utilizing a large number of states is expensive, difficult to implement, and consumes a lot of power.

Page 49, amend the paragraph beginning at line 11 as follows:

Figure 16 shows a sequence detector 1600-w having reduced complexity sequence detection. In particular, sequence detector 1600-w includes branch metric generator 1602-w, add-compare-select (unit) 1603-w, and starting point determiner 1605-w. Traceback 1604 and LIFO 1606 are coupled into sequence detector 1600-2 as well as similar detectors coupled to the remaining N wires. As an example, sequence detector 1600-w is shown for the PAM-5 alphabet, although embodiments of sequence detector 1600-w can utilize other symbol alphabets as well.

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Page 49, amend the paragraph beginning at line 22 as follows:

As mentioned above, the ~~The~~ PAM-5 symbol alphabet can be segregated into two families, an odd family X having the PAM-5 symbols {-1, +1} and an even family Y having the PAM-5 symbols {-2, 0, +2}. A detector state can now be defined as the previous η families X or Y, as opposed to the previous η PAM-5 symbols {-2, -1, 0, +1, +2}. Therefore, the number of states required for the PAM-5 symbol alphabet with η=2 ISI symbols is reduced from 25 states to 4 states on each transmission channel w=1 through L. For a four wire system (4-D decoding, for example), there are a total of sixteen (16) states instead of one hundred (100) states.

Page 50, amend equation 27, line 29, as follows:

In Figure 16, equalizer 1601-w can execute the transfer function

$$E(Z) = (1+\alpha_1 Z^{-1}+\alpha_2 Z^{-2})/f(Z). \quad \text{~~$E(Z) = (1+\alpha_1 Z^{-1}+\alpha_2 Z^{-2})/f(z).$~~} \qquad (27)$$

Therefore, the expected signal input to decoder system 1600 is

$$r_{k,w} = a_{k,w}+\alpha_1 a_{k-1,w}+\alpha_2 a_{k-2,w}. \qquad (28)\ \text{~~(27)~~}$$

Page 51, amend the paragraph beginning at line 17 as follows:

For each state S at k-1, symbols $\hat{a}_{k-1}(S)$and $\hat{a}_{k-2}(S)$ are known based upon feedback from ACS 1603-w to branch metric generator 1602-w ~~Branch Metric Generator 1602-W,~~ as ~~as is~~ shown in Figure 16. For each state transition S $\rightarrow$ S', branch metric generator takes the difference between the input signal and the ISI portion of Equation 28 ~~Equation 27~~ to obtain a difference

$$\sigma(S\rightarrow S') = r_{k,w} - \alpha_1 \hat{a}_{k-1,w}(S) - \alpha_2 \hat{a}_{k-2,w}(S). \qquad (29)\ \text{~~(28)~~}$$

The difference σ is then compared with the symbols for each possible branch of the state transition S to S'. The symbol $a'_{k,w}(S\rightarrow S')$ chosen for the branch ~~branch, $a'_{k,w}(S\rightarrow S')$,~~ is then assigned to the transition from state S to state S'.

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Page 51, amend the paragraph beginning at line 30 as follows:

With reference to ~~As is shown in~~ Figure 18, the ~~The~~ branch metrics can be computed for each transition S to S' according to the equation:

$$M_{k,w}(S\rightarrow S') = [r_{k,w} - a'_{k,w}(S\rightarrow S')- \alpha_1 \hat{a}_{k-1,w}(S) - \alpha_2 \hat{a}_{k-2,w}(S)]^2, \quad (30)\ (29)$$

where the valid transitions (S→S') in Figure 18 are S→S' = XXX, XXY, YXX, YXY, XYX, XYY, YYX and YYY. The notation "ABC" used above and in Figure 18, where each of "A", "B" and "C" is X or Y, ~~on Figure 18~~ indicates an S→S' transition from S=AB to S'=BC.

Page 52, amend the paragraph beginning at line 5 as follows:

Add-compare-select 1603-w receives the branch metrics $M_{k,w}((S\rightarrow S')$ and branch decisions $B_{k,w}(S\rightarrow S')$ from branch metric generator 1602-w and calculates the state metrics $P_{k,w}(S')$ according to the equation

$$P_{k,w}(S') = \min_{j=\{S\}}(P_{k-1,w}(j) + M_{k,w}(S\rightarrow S')), \quad (31)\ (30)$$

where j is equal to each S such that S→S' is allowable.

Page 52, amend the paragraph beginning at line 22 as follows:

The error $\Delta_{k,w}(S')$ is the difference in metrics between the two paths resulting in state S':

$$\Delta_{k,w}(S') = \left| M(S_1\rightarrow S')-M(S_2\rightarrow S') \right|, \quad (32)\ (31)$$

where S_1 is one of the two initial states that transition to the final state S' and S_2 is the other of the two initial states that transition to the final state S'. For example, from Figure 18, if S'=YX, then S_1 and S_2 are the states XY and YY, respectively.

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Page 53, amend the paragraph beginning at line 6 as follows:

Traceback circuit 1604 can be the same as traceback 1404 of Figure 15 except that read modules 1501-1 through 1501-4 receive a different set of parameters $\Gamma_{k,w}$. In traceback circuit 1604, $\Gamma_{k,w}$ includes the ACS parameters $D_{k,w}(S_i)$, $\Delta_{k,w}(S_i)$, $B1_{k,w}(S_i)$, $B2_{k,w}(S_i)$, where

S_i = (XX, XY, YX, YY), and the starting point $SP_{k,w}$ from starting point determiner 1605-w. As described above, read modules 1501-1 through 1501-4 store the ACS results in memory and, starting from starting point $SP_{k,w}$ determined by starting point determiner 1605, determine ~~determines~~ the most likely symbol $\hat{a}_{k,w}$ and the second most likely symbol $\hat{a}2_{k,w}$ for clock cycle k. A reliability ~~An reliability~~ measure $\varepsilon_{k,w}$ indicating the difference in distance metrics between the most likely symbol and the second most likely symbol ~~symbol, $\varepsilon_{k,w}$~~ is also determined.

Page 53, amend the paragraph beginning at line 21 as follows:

As is shown in Figure 15, read modules 1501-1 through 1501-4 output the parameters $\hat{a}_{k,w}$ to parity check 1502 and decoder 1504, parameters $\hat{a}2_{k,w}$ to decoder 1504, and parameters $\varepsilon_{k,w}$ to error analysis 1503. As was previously discussed, decoder 1504 outputs the ~~outputs a the~~ best symbols $\hat{a}'_{k,w}$ based on the parity check and informs read modules 1501-1 through 1501-4 of the choice. Read modules 1501-1 through 1501-4 then proceed to determine most likely and second most likely symbols for clock cycle k-1 until the traceback is complete.

Page 53, amend the paragraph beginning at line 31 as follows:

In sequence detector 1600-w of Figure 16, the minimum squared distance between parallel branches of any transition S→S' should be at least twice as large as the minimum squared distance of the overall decoder. Because there is no protection between parallel branch decisions S→S" of ~~decisions S → S" of~~ sequence detector 1600-w, this requirement on minimum squared distances should hold true in order to prevent the overall minimum distance from decreasing because of reduced state detection.

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Page 54, amend the paragraph beginning at line 24 as follows:

Figure 19 shows an example of a simplified decision feedback equalizer 1900. The simplified decision feedback equalizer includes a pre-equalizer section 1901, an adder 1902, a slicer 1903, and a feedback section 1905. ~~delays 1904 and 1905, and selector 1906.~~ Pre-equalizer section 1901 can be any equalizer structure that reduces the ISI length to L symbols. Pre-equalizer section 1901, therefore, executes the transfer function

$$T(Z) = \frac{1 + \alpha_1 Z^{-1} + \cdots + \alpha_L Z^{-L}}{f(Z)}, \qquad \underline{(33)}\ \sout{(32)}$$

where α_1 through α_L are the multiplier coefficients of pre-equalizer section 1901 and f(Z) is the response of the input channel (*see* Equation 2 for the response of a transfer channel).

Page 55, amend the paragraph beginning at line 5 as follows:

The output signal $\underline{a'_k}$ from <u>from pre-equalizer (or feedforward)</u> ~~feedforward~~ section <u>1901</u> ~~1901, a'_k,~~ is input to adder 1902. Adder 1902 subtracts the signal $\underline{a''_k}$ from selector <u>1906</u> ~~1906, a''_k,~~ from the output signal $\underline{a'_k}$ from feedforward section <u>1902.</u> ~~1902, a'_k.~~ The resulting <u>signal</u> ~~signal,~~ $a'''_k = a'_k - a''_k$ ~~, is~~ is input to slicer 1903. Slicer 1903 outputs a symbol $\hat{a}_k$ that is closest to the input signal a'''_k. The feedback section 1905 (see also feedback section 811 of Figure 8) of decision feedback equalizer 1900 comprises delays <u>1904-1 and 1904-L</u> ~~1904 and 1905~~ and selector 1906. Selector 1906 receives each of L past symbols $\hat{a}_{k-1}$ through $\hat{a}_{k-L}$ and uses these symbols to access a lookup table. The lookup table holds values ξ_1 through ξ_Q. The output signal $\underline{a''_k}$ of selector <u>1906</u> ~~1906, a''_k,~~ then is that one of ξ_1 through ξ_Q that corresponds to the combination of inputs $\hat{a}_{k-1}$ through $\hat{a}_{k-L}$. The time required to look the results up in a look-up table is much less than the time required to perform the L <u>mulltiplications</u> ~~multiplies~~ and L additions required of the feedback section shown, for example, as feedback section 811 of Figure 8.

Page 56, renumber equation 33, beginning at line 3 as follows:

As an example, in a system using the PAM-5 alphabet where L=2, and Q is 25 there are twenty-five (25) lookup values (i.e., Q=25). Because the intersymbol interference in the input signal to adder 1902 is the result of two (2) ISI symbols,

$$a'_k = a_k + \alpha a_{k-1} + \beta a_{k-2} + n_k, \qquad \underline{(34)}\ \sout{(33)}$$

where α and β are the interference parameters and n_k is random noise. The twenty-five values for the look-up table, therefore, are given by:

$a''_k = \xi_1 = 2\alpha+2\beta$ if $(\hat{a}_{k-1} = 2)$ and $(\hat{a}_{k-2} = 2)$;
$a''_k = \xi_2 = 2\alpha+\beta$ if $(\hat{a}_{k-1} = 2)$ and $(\hat{a}_{k-2} = 1)$;
$a''_k = \xi_3 = 2\alpha$ if $(\hat{a}_{k-1} = 2)$ and $(\hat{a}_{k-2} = 0)$;
$a''_k = \xi_4 = 2\alpha-\beta$ if $(\hat{a}_{k-1} = 2)$ and $(\hat{a}_{k-2} = -1)$;

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$a''_k = \xi_5 = 2\alpha-2\beta$ if $(\hat{a}_{k-1} = 2)$ and $(\hat{a}_{k-2} = -2)$;
$a''_k = \xi_6 = \alpha+2\beta$ if $(\hat{a}_{k-1} = 1)$ and $(\hat{a}_{k-2} = 2)$;
$a''_k = \xi_7 = \alpha+\beta$ if $(\hat{a}_{k-1} = 1)$ and $(\hat{a}_{k-2} = 1)$;
$a''_k = \xi_8 = \alpha$ if $(\hat{a}_{k-1} = 1)$ and $(\hat{a}_{k-2} = 0)$;
$a''_k = \xi_9 = \alpha-\beta$ if $(\hat{a}_{k-1} = 1)$ and $(\hat{a}_{k-2} = -1)$;
$a''_k = \xi_{10} = \alpha-2\beta$ if $(\hat{a}_{k-1} = 1)$ and $(\hat{a}_{k-2} = -2)$;
$a''_k = \xi_{11} = 2\beta$ if $(\hat{a}_{k-1} = 0)$ and $(\hat{a}_{k-2} = 2)$;
$a''_k = \xi_{12} = \beta$ if $(\hat{a}_{k-1} = 0)$ and $(\hat{a}_{k-2} = 1)$;
$a''_k = \xi_{13} = 0$ if $(\hat{a}_{k-1} = 0)$ and $(\hat{a}_{k-2} = 0)$;
$a''_k = \xi_{14} = -\beta$ if $(\hat{a}_{k-1} = 0)$ and $(\hat{a}_{k-2} = -1)$;
$a''_k = \xi_{15} = -2\beta$ if $(\hat{a}_{k-1} = 0)$ and $(\hat{a}_{k-2} = -2)$;
$a''_k = \xi_{16} = -\alpha+2\beta$ if $(\hat{a}_{k-1} = -1)$ and $(\hat{a}_{k-2} = 2)$;
$a''_k = \xi_{17} = -\alpha+\beta$ if $(\hat{a}_{k-1} = -1)$ and $(\hat{a}_{k-2} = 1)$;
$a''_k = \xi_{18} = -\alpha$ if $(\hat{a}_{k-1} = -1)$ and $(\hat{a}_{k-2} = 0)$;
$a''_k = \xi_{19} = -\alpha-\beta$ if $(\hat{a}_{k-1} = -1)$ and $(\hat{a}_{k-2} = -1)$;
$a''_k = \xi_{20} = -\alpha-2\beta$ if $(\hat{a}_{k-1} = -1)$ and $(\hat{a}_{k-2} = -2)$;
$a''_k = \xi_{21} = -2\alpha+2\beta$ if $(\hat{a}_{k-1} = -2)$ and $(\hat{a}_{k-2} = 2)$;
$a''_k = \xi_{22} = -2\alpha+\beta$ if $(\hat{a}_{k-1} = -2)$ and $(\hat{a}_{k-2} = 1)$;
$a''_k = \xi_{23} = -2\alpha$ if $(\hat{a}_{k-1} = -2)$ and $(\hat{a}_{k-2} = 0)$;
$a''_k = \xi_{24} = -2\alpha-\beta$ if $(\hat{a}_{k-1} = -2)$ and $(\hat{a}_{k-2} = -1)$;
$a''_k = \xi_{25} = -2\alpha-2\beta$ if $(\hat{a}_{k-1} = -2)$ and $(\hat{a}_{k-2} = -2)$. (35) ~~(34)~~

Page 57, amend the paragraph beginning at line 16 as follows:

Pre-equalizer section 2001 of sequence detector 2000 receives signal $y_{k,w}$, and executes a transfer function, such as that shown in Equation 33, ~~Equation 32,~~ that removes the ISI influence from all but L past symbols. Feedback section 2003 outputs a signal $a''_{k,w}$ that removes the influence from an additional M past symbols based on the inputs from the ACS. Sequence detector 2000 therefore utilizes~~, therefore, utilize~~ states describing the past L-M ISI symbols. Figure 12, for example, illustrates a trellis diagram for L-M = 1. Figures 17 and 18, for example, illustrate a trellis diagram for a reduced state sequence detector with L-M = 2.

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Page 57, amend the paragraph beginning at line 28 as follows:

As occurs in branch metric generators 1101, 1302, 1402-w, and 1602-w, ~~was described before,~~ branch metric generator 2004 outputs a set of branch metrics $M_k(S \rightarrow S')$ for transitions between states S and state S' of the decoder. ACS 2005 outputs the ACS results to traceback circuitry 2006, and the transition metrics to starting point 2007. Traceback circuit

2006 outputs the symbols decided by sequence detector 2000, in reverse chronological order, and LIFO 2008 reverses the order of those symbols to output symbol stream $\hat{a}_{k,w}$.

Page 58, amend the paragraph beginning at line 4 as follows:

From Figure 20A, ~~Figure 20,~~ if the past L symbols have been properly decoded than the influence of intersymbol interference will be completely canceled. In general, feedback section 2003 can be any feedback structure. An example feedback section is feedback section 811 shown in Figure 8. Feedback section 811, however, includes M multipliers (multipliers 806-1 through 806-M) and an M-input adder (adder 807) for the case of M ISI symbol cancellation.

Page 58, amend the paragraph beginning at line 13 as follows:

One embodiment of feedback section 2003 includes feedback sections like feedback section 811. For Gigabit Ethernet, at symbol rates of 125 Mhz on each wire, the timing constraints of the sequence detector are severe. When "per-survivor processing" (*see, e.g.*, sequence detector 1300 of Figure 13) is used, feedback ~~feed-back~~ section 2003 must include feedback section 811 repeated for each state of equalizer 2000 because the final state of equalizer 2000 is not determined until the latest decision of ACS 2005 (i.e., the parameters $S_{k,w}$ are determined by ACS 2005).

Page 58, amend the paragraph beginning at line 24 as follows:

Figure 20B shows an embodiment of feedback section 2003 that includes a look-up feedback section 2100. Look-up feedback section 2100 outputs an output signal a''_k from look-up values ξ_1 through ξ_Q in response to the ACS parameters S_{k-1} through S_{k-L}. Look-up values ξ_1 through ξ_Q can be preloaded into feedback section 2100 or may be periodically adaptively chosen and read into feedback section 2100. Values for look-up values ξ_1 through ξ_Q for two ISI symbols and a PAM-5 symbol alphabet are given above in Equation 35. ~~Equation 34.~~

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Enclosed is a substitute specification that incorporates all of the preceding revisions to the specification. The page numbers of the substitute specification begin with the letter "S" to help distinguish the substitute specification from the specification as originally filed. Further enclosed is a copy of the original specification annotated in red to indicate all of the preceding changes to the specification.

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